

Notice of References Cited	Application/Control No. 10/586,176		Applicant(s)/Patent Under Reexamination KOHLER ET AL.	
	Examiner FERNANDO N. HIDALGO		Art Unit 2827	Page 1 of 1

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	B	US-			
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	J	US-			
	K	US-			
	L	US-			
	M	US-			

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	N	WO 2004053886 A1	06-2004	World Intellect	REINER, JOACHIM CHRISTIAW	
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	U	Doyle et al., Characterization of oxide trap and interface trap creation during hot-carrier stressing on n-mos transistors using the floating-gate technique, 1993, IEEE Electron Device Letters, Vol. 14, No. 2, February 1993; all pages.
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.